REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

Claim 1 has been amended to require the recess to have a substantially closed perimeter and an inner wall surface that supports the component/electrical interconnect structure assembled thereinto.

This, in part, incorporates wording previously found in claim 54, which has therefore been cancelled without prejudice or disclaimer. New claim 55 requires that the packaging layer is otherwise substantially continuous.

Amendments to claim 1 are based on all the embodiments described and shown in the figures. In all the figures showing assembled components, there is one or more recess (500, 505, 510, 515, 525) in the packaging layer (200, 1700). Every recess necessarily has a supporting sidewall surface within it.

These recesses are formed in a layer whose primary purpose is packaging and the recesses contribute to that packaging role. They receive and support components or interconnect material for the components. The sidewall surfaces of the recesses necessarily provide support in a lateral direction (as can be seen in the figures) because the components and interconnect material fit snugly into them.

The rejection of claims 1, 14, 21-23, 29, 38-42, 45 and 54 under 35 U.S.C. §103 as allegedly being made "obvious" based on Tanisawa '778 in view of Iha '429 is respectfully traversed.

Applicant's previous comments of record concerning deficiencies of both of these references are hereby incorporated by reference so as not to unduly burden the present record.

The Examiner is thanked for providing a "response to arguments" section explaining why applicant's arguments of June 23, 2010, were not found persuasive. The Examiner is respectfully requested to reconsider these responsive comments in light of the following additional comments (and hopefully a restudy of applicant's earlier comments of June 23, 2010).

The Examiner's own discussion of Tanisawa admits that Tanisawa does not refer to the "insulating layer 33" as constituting a "packaging layer". Indeed, the undersigned has been unable to find any description in Tanisawa of any structure therein described as being a "packaging layer".

The Examiner notes that Tanisawa describes each of the solder bumps 23 to be surrounded by sidewalls 32 defined by an insulating layer 33 (4:56-59) – and then asserts that such surrounding sidewalls support the semiconductor chip 5, relying upon Tanisawa at 5:45-60. However, all of the Figs. 5A-5C being described at col. 5 clearly show substantial gaps between the solder bumps 23 and the sidewalls 32 of the insulating layer 33. It is true that Fig. 5B does show a horizontally displaced semi-

conductor chip 5 as it is in the process of being lowered into place onto molten solder bumps 23. In this transitory context, the molten solder bumps do appear in Fig. 5B to touch the upper corner of respective sidewalls 32 of insulating layer 33. However, it is clear from the description of Fig. 5B at 5:27-38, and common knowledge of those in the art having elementary physics understanding, that it is the surface tension of the molten solder bumps 23 that will ultimately move the semiconductor chip horizontally in the direction of arrow A so as to align the respective contact points 21, 22. See, for example, the explicit teaching at 5:34-35 that it is the molten solder bumps 23 that serve to horizontally move the optical semiconductor chip 5.

Once the semiconductor chip 5 is in the correct position (as determined by molten solder bump surface tension) and the solder bumps 23 have solidified, the arrangement depicted in Fig. 5C shows that the sidewalls 32 of the insulating layer 33 serve no support function whatsoever – with respect to either the solder bumps 23 or the chip 5.

Instead, as explicitly taught by the text at 5:45-60 cited by the Examiner, it is only the top surface of a small plateau of insulating layer 33 (in the middle of the asserted "recess") that comes into contact with the bottom surface of chip 5, thus keeping it at the proper vertical height.

As will be appreciated by careful study of column 5 and Figs. 5A-5C, the insulating layer 33 does not have any sidewall capable of providing lateral support to semiconductor chip 5. Instead, it is only the solidified solder bumps 23 that restrain horizontal movements.

The Examiner apparently recognizes this deficiency vis-à-vis chip 5, but then switches gears to argue that the insulating layer 33 provides both support and protection of the inter-connect features 23 (i.e., solder bumps 23). However, in the assembled configuration of Fig. 5C, the insulating layer 33 is clearly not in contact at all even with solder bumps 23. Indeed, the Tanisawa discussion of prior art Figs. 2A-2C appearing in cols. 3-4 do not talk about a problem in self-alignment in the horizontal dimension, but instead refer to the conventional method as being disadvantageous in that the solder bumps 23 should be controlled in their vertical heights (e.g., see 4:1-5).

However, while an isolated plateau of insulating layer 33 in Figs. 5A-5C may de-limit the minimum vertical dimension permitted by the solidified solder bumps 23, the insulating layer 33 does not serve to support the solder bumps 23 at all.

Indeed, with respect, it is noted that the Examiner's comments subtly shift between talking about the chip 5 and the interconnect features (solder bumps) 23. Applicant's claims are directed to assembly of components or an electrical interconnect structure therefore – but one must at least consistently consider one or the other (or both together)

rather than shifting between such structures when making comparisons to the claimed subject matter as a whole.

The Examiner's discussion of the applicant's packaging layer 200 in Fig. 12 is of interest because the Examiner there apparently recognizes that the applicant's packaging layer 200 as depicted in Fig. 12 surrounds (and supports) interconnecting mounting pad components 1200. It is also respectfully noted, however, that Fig. 12 depicts solder bumps 1205 as extending on top of mounting pads 1200. Accordingly, contrary to the Examiner's comments, Tanisawa's insulating layer 33 having walls 32 loosely surrounding (but not supporting) each of the solder bumps 23 is actually not so similar to the applicant's packaging layer 200 depicted in Fig. 12.

The Examiner's comments go on to assert that the Tanisawa recesses within insulating layer 33 are similar to the recesses within applicant's packaging layer 200 as shown in Fig. 7 – where the Examiner asserts that there are complete breaks or gaps exposing the principal surface of substrate 100. However, the Examiner is respectfully reminded that Fig. 7 depicts cross-section A-A from Fig. 6 – and the lithographically defined holes (i.e., recesses) in the packaging layer 200 as depicted in Fig. 7 are intended to receive and support various components 500, 505, 510 and 515 thereinto (e.g., see page 20, line 27, et seq. of the applicant's specification). Accordingly, once again, the Examiner's assertions of similarity are actually not supported by the factual record.

The Examiner asserts that Tanisawa's disclosed insulating layer material (silica) is a "well known packaging material in the semiconductor art". However, the Examiner offers no factual support for this assertion – and, in any event, this ignores the fact that applicant's claims require the packaging layer to comprise a hybrid glass material having both organic and inorganic components – which material has particular benefits (e.g., see the specification at page 19, lines 22-32).

The Examiner's assertion that the combined teachings of Tanisawa and Iha "read on all the structural limitations of the claim" is also respectfully traversed – both for reasons noted in applicant's remarks of June 23, 2010, and as further detailed above and below.

The Examiner cites case law without any explanation of the factual context involved therein and how that might compare to the present factual context – and cites to MPEP §2112.01 for the proposition that a prima facie case of either anticipation or obviousness may be established when prior art products are identical or substantially identical in structure or composition or are produced by identical or substantially identical processes (vis-à-vis the claimed subject matter).

However, the Examiner ignores the material structural differences (as already noted) and omits reference to the fact that this same section of the MPEP notes that any such prima facie case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product.

By contrast, here, it has already been repeatedly noted that the prior art does not even provide a substantially identical structure (or composition). Nor has the Examiner demonstrated any prior art that assembles at least one optical component and at least one different component for use together as an assembly carried by a substrate and assembled into a packaging layer also carried by the substrate, the packaging layer comprising hybrid glass material having both organic and inorganic components and being provided with at least one recess for use in assembling such components, the having a wall surface therewithin supporting the at least one assembled optical component or electrical interconnect therefor, said recess having a perimeter that is substantially closed into which the component or electrical interconnect structure therefor is assembled.

For example, the Examiner has not indicated how a silica insulating layer can possibly have a substantially identical composition, structure and/or function as the applicant's recited hybrid glass material packaging layer. Nor has the Examiner even found a substantially identical structure for reasons already of record or herein made of record. Accordingly, it is respectfully maintained that the Examiner has not yet defined even a prima facie case of "obviousness" – including the required Graham v. Deere factual analysis under Section 103.

This filling characteristic of the packaging layer allows it to provide the common functions of a packaging layer, including planarization, protection and support to the component(s) for handling and processing.

Layers that are used for their electrical characteristics, such as insulating layers, need only be provided where insulation is required. They are not intended for the purpose of packaging, although they may arguably sometimes make a packaging contribution.

The electrically insulating layer of Tanisawa is an excellent example of a layer put down primarily for a different purpose, in this case, electrical. The "recesses" shown in Tanisawa are solely to give access to electrical connections as the recesses themselves play no part in packaging at all. As can be seen in Fig. 5C, the internal walls of the recesses in Tanisawa are clear of contact with anything else at all. The wall surfaces inside the recesses cannot provide a supporting role.

There is support provided for assembled components in the construction of Tanisawa, but it is provided by the solidified solder bumps and/or the top of a small plateau of insulating material 33 provided within the "recesses". That vertical support could be constructed as an island of insulating material, or a broad post, and still provide the necessary vertical support.

It is also clear, again from Fig. 5C in Tanisawa, that the insulating layer 33 and the "recesses" are not intended to have a substantial packaging role since the "recesses" leave gaps underneath the component and indeed around it in the assembled construction.

Indeed, the Tanisawa components are not shown in a "packaged" form at all in the normal sense as understood in semiconductor technology.

If the insulating material of Iha were to be substituted for the insulating material of Tanisawa, one would still have the components supported on an insulating layer, and the recesses would still provide no support at all in packaging.

With respect to the withdrawn claims, it is respectfully requested that at least claims 2-13, 15-20, 24-28, 30-37, 43 and 44 be rejoined since they are clearly species of the allowable elected claims (e.g., because they depend directly or indirectly therefrom). It is also respectfully requested that method claims 46-53 be rejoined since they depend from and thus incorporate all limitations of elected parent claim 1.

Accordingly, this entire application is now believed to be in allowable condition, and a formal notice to that effect is earnestly solicited.

Respectfully submitted,

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